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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,882	07/17/2003	Hem P. Takiar	SAND-01004US0	3084
64948 7590 02/26/2008 VIERRA MAGEN/SANDISK CORPORATION 575 MARKET STREET SUITE 2500 SAN FRANCISCO, CA 94105				
EXAMINER				
CHANG, RICK KILTAE				
ART UNIT		PAPER NUMBER		
3726				
MAIL DATE		DELIVERY MODE		
02/26/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

10/621,882

Applicant(s)

TAKIAR, HEM P.

Examiner

Rick K. Chang

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 52-90 is/are pending in the application.
- 4a) Of the above claim(s) that are not listed in item 6 below is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 52-60-71, 73, 75, 76, 78, 80-82, 86 and 88-90 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-949)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(c), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(c) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/26/07 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 60-63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The disclosure, as originally filed, failed to provide support for "said step of covering includes applying a film directly to a first surface of said circuit board" (claim 60, lines 2-3). The disclosure states applying a conformal contact coating to cover the test terminals, not two layers (a conformal contact coating and a film) covering the test terminals.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 60-63, 76, 78, 80-82 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 60, line 2: is “a film” referring to “a conformal contact coating” or some other film? Is covering step require one layer (a conformal contact coating) or two layers a conformal contact coating and a film)?

Claim 61, line 2: What is “one surface” referring to?

Claims are ambiguous and competitors would be unable to discern the bounds of the invention.

Claim 76, line 3: Is “circuit boards” referring to “a plurality of circuit boards” or something else?

Claim 76, line 5: “said connected circuit boards” lacks positive antecedent basis.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 52, 60-61, 68-70, 76, 80, 86, 88 and 90 are rejected under 35 U.S.C. 102(a) as being anticipated by Corisis et al (US 6,462,273).

Re claims 52 and 86: Corisis discloses adding circuit elements (14) to a circuit board (12), said circuit board includes a set of test terminals (36); testing one or more of said circuit elements using said test terminals (col. 4, lines 30-34); and covering said test terminals with a

conformal contact coating in order to prevent access to said test terminals (Figure 3D shows the circuit board and contacts covered with molded plastic 18 (which can broadly be considered the claimed "conformal contact coating" that prevents access to the testing contacts 36).

Re claims 60 and 88, as best understood: Corisis discloses said step of covering includes applying a film (16 and 18) directly to a first surface of said circuit board or a peripheral card.

Re claim 61, as best understood: Corisis discloses that said film includes an adhesive (18 is an epoxy) on one surface (12 or 16).

Re claim 68: Corisis discloses that said circuit board (12) includes a conductive layer and a first portion of said conductive layer forms said test terminals (36 in Fig. 1G).

Re claim 69: Corisis discloses that a second portion of said conductive layer forms user terminals (34); said user terminals are positioned on an outside surface of said memory card (where 34 lies on 12); and said user terminals are in communication with at least a subset of said circuit elements (44).

Re claim 70: Corisis discloses said step of adding circuit elements includes performing a transfer mold process to encapsulate said circuit elements without covering said test terminals (16 is formed using transfer molding process; see Fig. 2B).

Re claim 76, as best understood: Corisis discloses adding circuit elements (14) to a circuit board (12), said circuit board includes a set of test terminals (36); testing one or more of said circuit elements using said test terminals (col. 4, lines 30-34); and covering said test terminals with a conformal contact coating in order to prevent access to said test terminals (Figure 3D shows the circuit board and contacts covered with molded plastic 18 (which can broadly be considered the claimed "conformal contact coating" that prevents access to the testing contacts

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36). Corisis discloses providing a strip containing multiple PCBs, encapsulating the PCBs and singulating PCBs from the strip.

Re claim 80, as best understood: see claim 60.

Re claim 90: Corisis discloses a memory card (col. 1, lines 23-25).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 62, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al (US 6,462,273) in view of Schwenck et al (US 7,065,656).

Corisis fails to disclose that said film includes mylar.

Schwenck discloses that said film includes mylar (114 and 116).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Corisis by said film includes mylar, as taught by Schwenck, for the purpose of providing flexible encapsulant.

10. Claim 63, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al (US 6,462,273) in view of Courtenay et al (US 6,445,060).

Corisis fails to disclose that said film includes polyimide.

Courtenay discloses that said film includes polyimide (46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Corisis by said film includes polyimide, as taught by Courtenay, for the purpose of providing adhesion promoting material and encapsulant..

11. Claims 64-67, 81, as best understood, and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al (US 6,462,273) in view of Chhor et al (US 6,843,421).

Corisis fails to disclose said step of adding circuit elements includes adding a flash memory array to said circuit board, said step of adding circuit elements includes mounting a first die on said circuit board and mounting a second die on said first die, said first die includes a flash memory array and said second die includes a controller and said first die is wire bonded to said circuit board; and said second die is wire bonded to said circuit board.

Chhor discloses said step of adding circuit elements includes adding a flash memory array (30a and 30b) to said circuit board (Figs. 1-2), said step of adding circuit elements includes mounting a first die on said circuit board and mounting a second die on said first die (Fig. 11), said first die includes a flash memory array (30b) and said second die includes a controller (30a), and said first die is wire bonded to said circuit board; and said second die is wire bonded to said circuit board (Fig. 11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Corisis by said step of adding circuit elements includes adding a flash memory array to said circuit board, said step of adding circuit elements includes mounting a first die on said circuit board and mounting a second die on said first die and said first die includes a flash memory array and said second die includes a controller, as taught by Chhor, for the purpose of forming semiconductor memory encased within a molded resin to form a memory module.

12. Claims 71 and 78, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al (US 6,462,273) in view of Yamamoto et al (US 6,733,954).

Corisis discloses providing a strip containing multiple PCBs, encapsulating the PCBs and singulating PCBs from the strip. Corisis fails to disclose said step of covering is performed after said circuit board is removed from a strip of circuit boards.

Yamamoto discloses said step of said step of covering is performed after said circuit board is removed from a strip of circuit boards(Figs. 9-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Corisis by said step of covering is performed after said circuit board is removed from a strip of circuit boards, as taught by Yamamoto, for the purpose of protecting the PCB from the environment, such as debris from the singulating process performed after encapsulating.

13. Claims 73, 75 and 82, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al (US 6,462,273) in view of Chhor et al (US 6,843,421).

Corisis discloses said step of covering includes applying a film (16 and 18) directly to a first surface of said circuit board. Corisis fails to disclose that the memory card is a flash memory card.

Chhor disclose that the memory card is a flash memory card (col. 3, lines 1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Corisis by the memory card is a flash memory card, as taught by Chhor, for the purpose of easily erasing and reprogramming the memory card.

Conclusion

14. Please provide reference numerals (either in parentheses next to the claimed limitation or in a table format with one column listing the claimed limitation and another column listing corresponding reference numerals in the remark section of the response to the Office Action) to all the claimed limitations as well as support in the disclosure for better clarity (optional). Applicants are duly reminded that a full and proper response to this Office Action that includes any amendment to the claims and specification of the application as originally filed requires that the applicant point out the support for any amendment made to the disclosure, including the claims. See 37 CFR 1.111 and MPEP 2163.06.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rick K. Chang whose telephone number is (571) 272-4564. The examiner can normally be reached on 5:30 AM to 1:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Bryant can be reached on (571) 272-4526. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Rick K. Chang/

Primary Examiner, A.U. 3726

RC

February 26, 2008